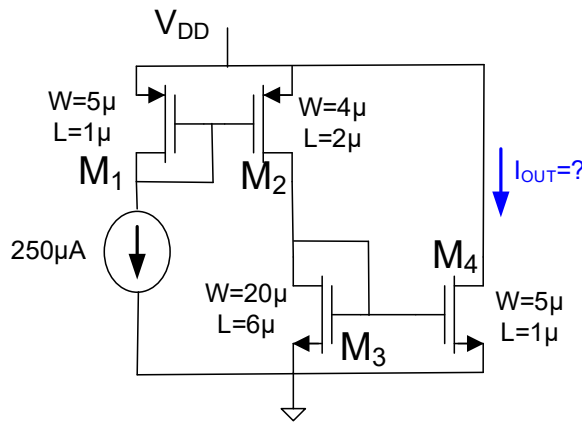


Solve Problems 1 – 10. The remaining problems are practice problems and will not be collected. Unless specified to the contrary, assume all n-channel MOS transistors have model parameters  $\mu_n C_{OX} = 250 \mu A/V^2$ ,  $V_{Tn} = 0.4V$ , all p-channel transistors have model parameters  $\mu_p C_{OX} = \mu_n C_{OX} / 3$ ,  $V_{Tp} = -0.4V$ , and all JFET devices are from a process with  $I_{DSSn0} = 100 \mu A$ ,  $I_{DSSp0} = 30 \mu A$ ,  $V_{Pp} = 1V$ ,  $V_{Pn} = -1V$ , and  $\lambda = 0$ . In this process, assume that for all MOS devices,  $L_{MIN} = W_{MIN} = 0.18 \mu m$ , and  $V_{DD} = 2V$ . Assume also that a bipolar process is available with parameters  $J_S = 10^{-14} A/\mu^2$  and  $\beta_n = 100$  and  $\beta_p = 40$ . Unless stated to the contrary, assume the output conductance of the BJT and the MOSFET are characterized, respectively, by  $V_{AF} = 100V$  and  $\lambda = .01V^{-1}$ .

**Problem 1** Determine  $I_{OUT}$ . Assume  $V_{DD} = 2V$ .



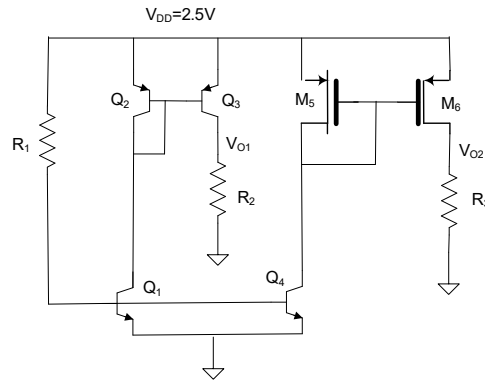
**Problem 2** Assume you have available a supply voltage of  $V_{DD} = 2V$  and a 5mA sourcing current (one end connected to  $V_{DD}$ ).

- Design a current mirror that provides two outputs, a sinking current of 100uA and a sourcing current of 10mA to load resistors  $R_{L1}$  and  $R_{L2}$  using MOS transistors.
- What is the maximum voltage for the 10mA sourcing current source for your design if it is to work as a current mirror.

**Problem 3** Design a noninverting amplifier with a nominal gain of +5 that has an input impedance that is between 50K and 100K that can drive a 2K resistive load with one terminal of the load connected to ground. In this design you may use any number of MOS transistors, resistors, capacitors, and one dc voltage source. Verify your design analytically and with SPICE.

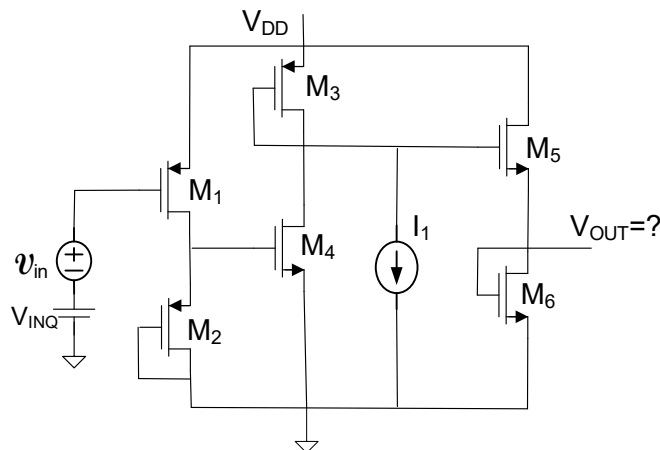
**Problem 4** Assume the MOS transistors are all operating in the saturation region and the Bipolar transistors are all operating in the Forward Active region.

- Determine the output voltages  $V_{O1}$  and  $V_{O2}$  in terms of the MOS device dimensions,  $W$  and  $L$ , the emitter areas, and the resistor variables  $R_1$ ,  $R_2$ , and  $R_3$ .
- If  $R_1 = 60K$ ,  $A_{E1} = A_{E2} = 100 \mu^2$ ,  $A_{E3} = 25 \mu^2$ ,  $A_{E4} = 300 \mu^2$ ,  $W_5 = 10 \mu m$ ,  $L_5 = 1 \mu m$ ,  $W_6 = 16 \mu m$ ,  $L_6 = 4 \mu m$ , Determine  $R_2$  and  $R_3$  so that  $V_{O1} = 2V$  and  $V_{O2} = 1V$ .

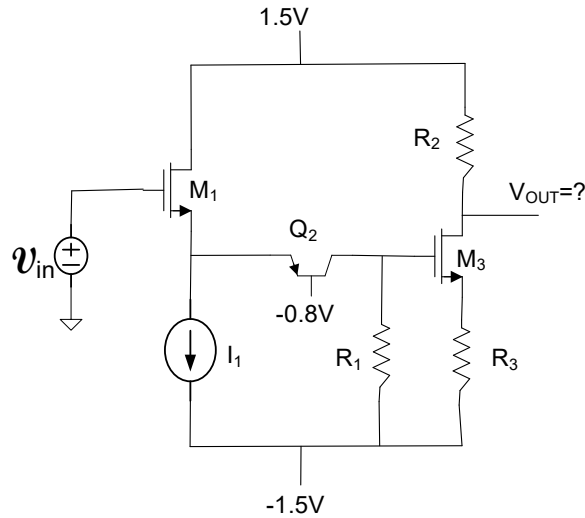


**Problem 5** Consider the following amplifier structure designed in a process with  $\mu_n C_{OX}=250\mu A/V^2$ ,  $\mu_p C_{OX}=\mu_n C_{OX}/3$ ,  $V_{THn}=0.4V$  and  $V_{THp}=-0.4V$ .

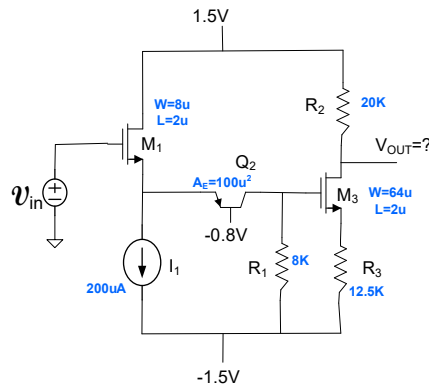
- Assuming all devices are operating in the saturation region, determine the small signal voltage gain in terms of the small-signal model parameters of the transistors.
- Assume  $V_{DD}=2V$ ,  $I_1=500\mu A$ , and the quiescent current in transistors  $M_1, M_4$ , and  $M_5$  is  $500\mu A$ . Numerically determine the small signal voltage gain if the quiescent voltage on the gate of  $M_4$  is  $1V$ , the voltage on the gate of  $M_5$  is  $1.3V$ , and the quiescent output voltage is  $0.7V$ . Be sure to use the model parameters given at the top of page 1 when solving this problem.



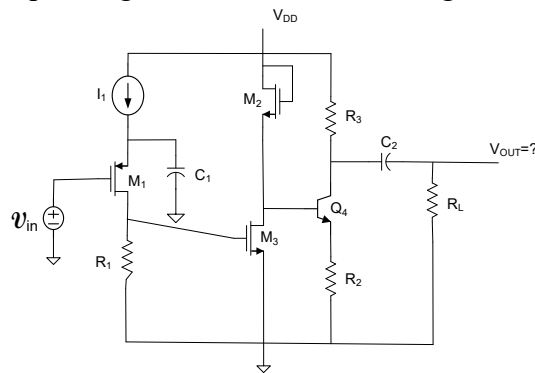
**Problem 6** Determine the small signal voltage gain in terms of the small signal model parameters of the devices. Assume the MOS transistors are operating in the saturation region and the bipolar transistor is operating in the forward active region. Assume the MOS transistors are from a CMOS process with  $\mu_n C_{OX}=250\mu A/V^2$ ,  $\mu_p C_{OX}=\mu_n C_{OX}/3$ ,  $V_{TNO}=0.4V$ , and  $V_{TP0}=-0.4V$ .



**Problem 7** If the component values for the circuit in the previous problem are as shown below, numerically determine the small-signal voltage gain. Assume the MOS transistors are in a 40nm CMOS process with  $\mu_n C_{OX}=250\mu A/v^2$ ,  $\mu_p C_{OX}=\mu_n C_{OX}/3$ ,  $V_{TNO}=0.4V$ , and  $V_{TP0}=-0.4V$ .



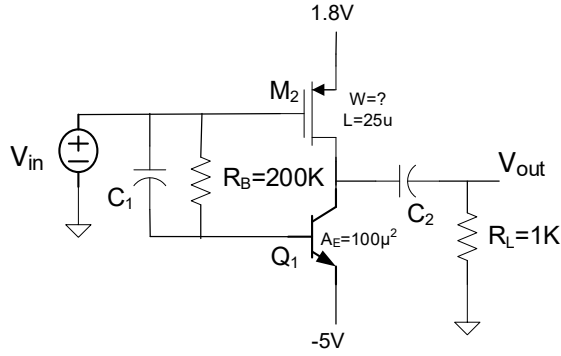
**Problem 8** Determine the small signal voltage gain in terms of the small signal model parameters of the devices. Assume the MOS transistors are operating in the saturation region and the bipolar transistor is operating in the forward active region.



**Problem 9** Design a noninverting amplifier using Bipolar transistors with a nominal voltage gain of 60 that has an input impedance larger than 100K and that can drive a 1K load resistor with one terminal of the load resistor connected to ground. You may use any number or resistors and capacitors in your design and a single 12V dc voltage source. Verify your design analytically and with SPICE.

**Problem 10** Consider the circuit shown below. Assume the width of  $M_2$  is selected so that the quiescent collector voltage of  $Q_1$  is 0V and assume the capacitors  $C_1$  and  $C_2$  are large.

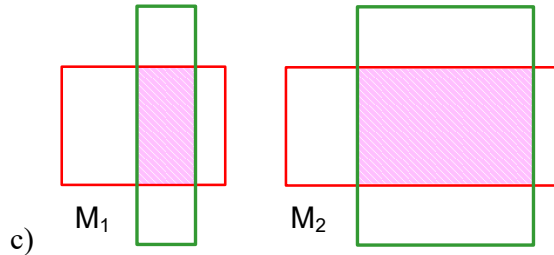
- a) Determine the small signal voltage gain in terms of the small-signal model parameters and the resistor values in the circuit.
- b) Determine the voltage  $v_{OUT}$  if  $v_{in}=0.01\sin 1000t$ .



**Problem 11** A potential layout strategy for a basic current mirror is shown below where the mirror gain is determined by the W/L ratio of the layout on the right to the W/L ratio of the layout on the left. If an n-channel current mirror is designed using this layout approach with an

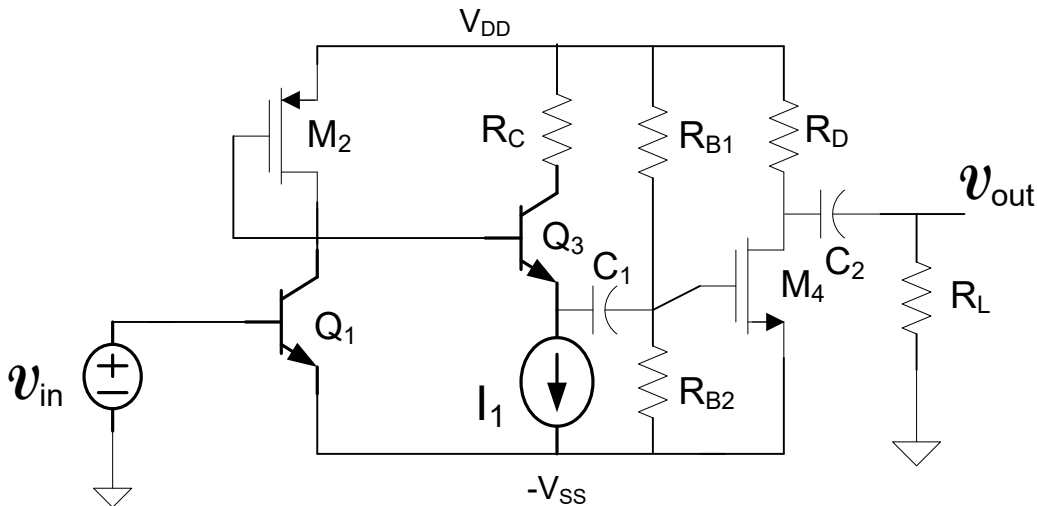
ideal mirror gain of  $M = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}}$  and with nominal values of  $L_1=L_2=4\mu$  and  $W_1=2\mu$ ,

$W_2=10\mu$ , determine the actual mirror gain if the field oxide encroachment into the active region results in an inward movement of the edges of  $0.1\mu$ .



**Problem 12** Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

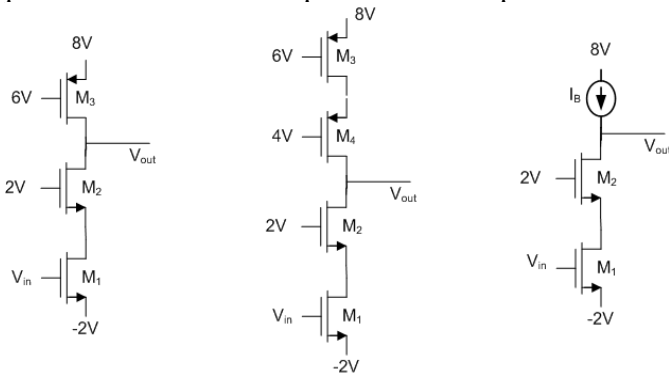
- Draw the small signal equivalent circuit.
- Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components



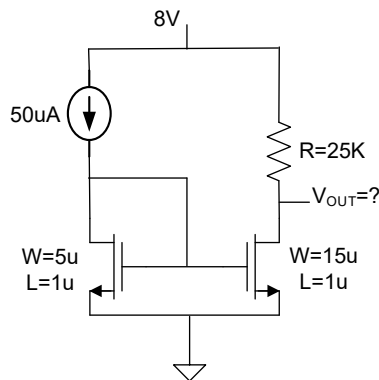
**Problem 13** Assume you have available a 2mA sourcing current (one end connected to  $V_{DD}$ ) and a single dc voltage source,  $V_{DD}$ .

- Design a current mirror that provides a sinking current of 200uA using MOS transistors.
- What is the minimum voltage of the 200uA current source in your design for it to still work as a current mirror.

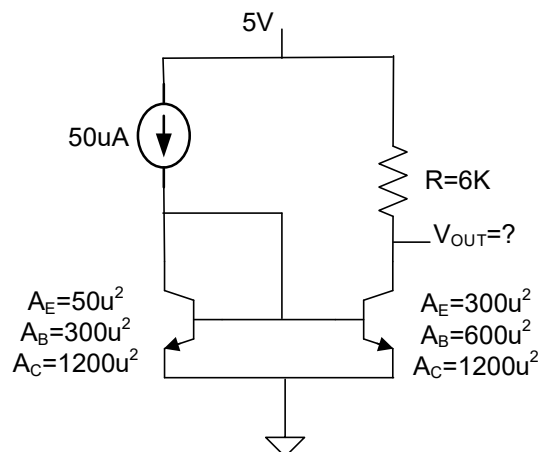
**Problem 14** Assume the following circuits are all sized and biased so that all transistors are in the saturation region. Determine the small signal voltage gain in terms of the small signal device parameters and make a quantitative comparison of the relative gains of the three circuits



**Problem 15** Determine  $V_{OUT}$ .



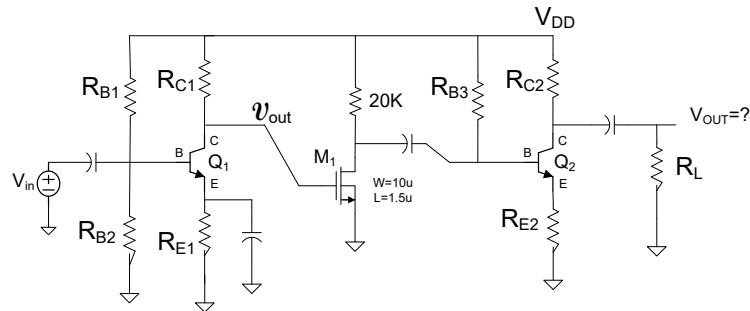
**Problem 16** Determine  $V_{OUT}$ .



**Problem 17** Design a current generator circuit that has output sinking currents of 10uA and 50uA. You have available MOS transistors, one resistor of value 200K, and a 5V dc voltage source.

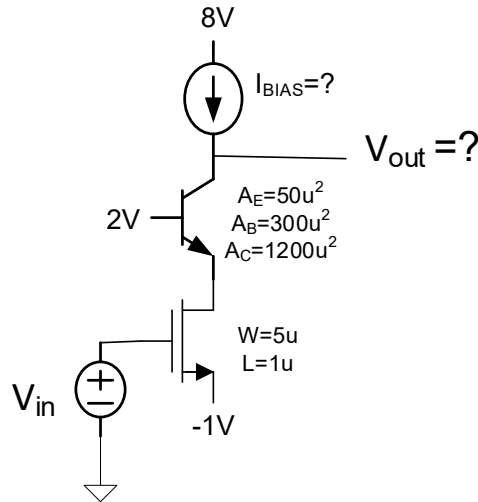
**Problem 18** Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

- Draw the small signal equivalent circuit.
- Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components
- Express the small signal voltage gain in terms of the quiescent values of  $I_{C1}$ ,  $I_{D1}$ ,  $I_{C2}$ , and the device model parameters (i.e. no small-signal parameters)



**Problem 19**

- If the current  $I_{BIAS}$  is selected so that the quiescent output voltage is 4V, determine the small signal voltage gain of this circuit.
- What is the approximate value of  $I_{BIAS}$  needed to establish  $V_{OUTQ}=4V$ ?



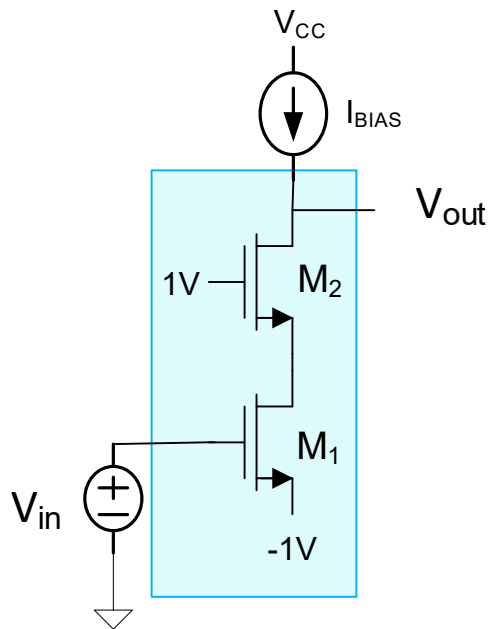
**Problem 20** US Patent 5,952,884 describes a new current mirror. It is pictured on the first page of the patent.

- What benefits do the inventors claim this current mirror has
- Provide an analytical development that verifies the claims the inventors make

**Problem 21** Identify one US patent that has been issued since 2002 that introduces a new current mirror. Give the current mirror schematic that is in the patent you identify and list the benefits the inventors claim this current mirror has.

**Problem 22** Consider the following circuit where  $M_1$  and  $M_2$  are matched with  $W=10\mu$  and  $L=2\mu$ .

- Determine  $I_B$  so that the quiescent output voltage is 4V.
- If the bias current obtained in Part a) were to change by .001%, how much change would occur in the quiescent output voltage?
- Obtain an expression for the small-signal voltage gain in terms of the small-signal model parameters.
- Determine a numerical value for the small-signal voltage gain.



**Problem 23-25** Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

- Draw the small signal equivalent circuit.
- Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components.

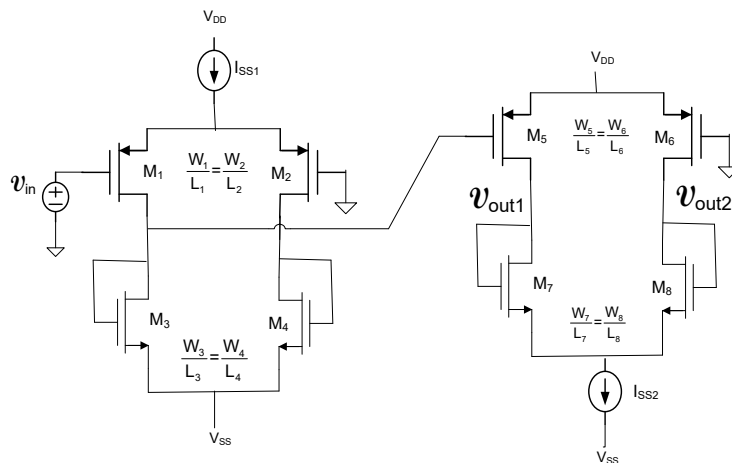
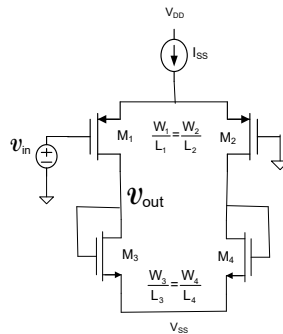
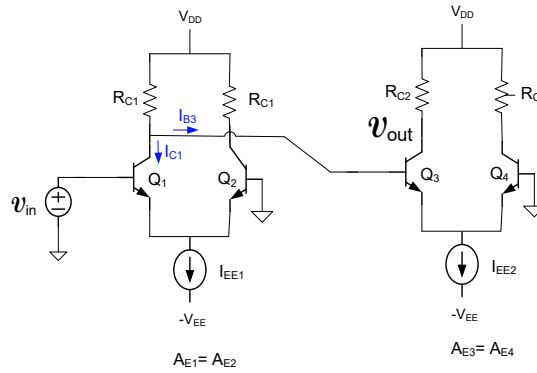
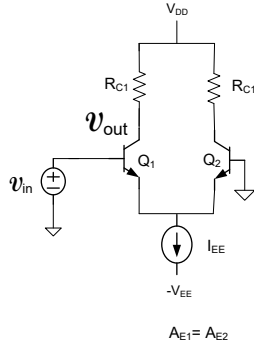




**Problem 26-29**

Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

- Draw the small signal equivalent circuit.
- Determine an expression for the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the passive components. The last circuit has two outputs so there are two voltage gains for this circuit.



**Problem 30** Use Modelsim to create a 4-bit shift register using the D flip-flops from the previous homework. The register should only change its value on a positive clock edge and include an enable bit. Create a test bench to test the correct operation of the shift register. Show multiple examples of loading and shifting. Include screenshots of your Verilog code, and simulation waveforms.